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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,081	12/23/2003	Yoshiyuki Nagatomo	246940US2	8110
22850	7590	05/19/2006	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			NGUYEN, HOA CAO	
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/743,081

Applicant(s)

NAGATOMO ET AL.

Examiner

Hoa C. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 07 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. The amendment filed on 3/7/06 has been entered.

#### *Drawings*

2. The amended drawings, figure 2 and 3, filed on 3/7/06 are not approved. Since these figures are prior art as disclosed in the specification, page 6, last 4 lines, therefore they must be labeled as -- Prior Art --, not -- Background Art --.

#### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being anticipated by Ninomiya et al. (US 5981085).

**Regarding claim 1**, as shown in figure 3, Ninomiya et al. disclose a heat-conducting multilayer substrate comprising at least a copper circuitry layer (no number)

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and a ceramic layer 8 (alumina is a ceramic material, column 7, lines 45-51). But, Ninomiya et al. does not clearly show the copper having 99.999% in purity.

However, Ninomiya et al. disclose a multiple of test results (see examples, from column 12) in which at least in one case copper particle of 99.99% purity is used. These examples and test results suggest that it is merely a matter of choice in selecting a particular copper depending on a specific application and a selection of the best suitable material involves only routine skill in the art.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select copper of at least 99.999% purity in order to maximize the electrical conductivity of the circuitry layer. Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

**Regarding claims 2-3**, as shown in figure 4, Ninomiya et al. disclose a heat-conducting multilayer substrate comprising:

- (a) A ceramic layer 8 (see claim 1 above);
- (b) a copper circuitry layer having a selectivity of at least 99.999% purity (see claim 1 above) provided on one side of the ceramic layer (the side where semiconductor device 7 connected to);
- (c) a metal layer 9 (metal film of copper, column 8, lines 1-5) provided on the other side of the ceramic layer.

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But, Ninomiya et al. does not disclose the copper circuitry layer having at least 99.999% purity or the metal layer 9 being a high-purity metal layer (a Cu metal of at least 99.999% purity).

As clearly explain in claim 1 above, a selection of the best suitable material involves only routine skill in the art.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select copper of at least 99.999% in purity in order to maximize the electrical conductivity of the circuit layer and also to maximize the thermal conductivity of the metal layer. Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

**Regarding claim 4**, as shown in figure 4, Ninomiya et al. disclose a power module substrate comprising:

- (a) An insulating substrate 8 (see claim 1 above);
- (b) a circuitry layer (no number, electrically connected to semiconductor device 7) laminated on one side (top side) of the insulating substrate 8 (see claim 2 above);
- (c) a metal layer 9 (column 8, lines 1-5) laminated on the other side of the insulating substrate (see claim 3 above);
- (d) a semiconductor chip 7 loaded onto the circuitry layer by means of solder (see column 13, lines 17-20);
- (e) a radiator 1 (composite substrate, column 5, line 55) joined to the metal layer.

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But, Ninomiya et al. does not disclose the circuitry layer and the metal layer are composed of copper having at least 99.999% in purity.

As clearly explain in claim 1 above, a selection of the best suitable material involves only routine skill in the art.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select copper of at least 99.999% in purity in order to maximize the electrical conductivity of the circuitry layer and also to maximize the thermal conductivity of the metal layer. Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

**Regarding claim 5**, Ninomiya et al. disclose the radiator 1 is joined to the metal layer 9 by solder, see column 8, lines 57-61.

**Regarding claims 6 and 7**, Ninomiya et al. disclose the insulating substrate is composed of alumina, which is  $\text{Al}_2\text{O}_3$ .

**Regarding claims 8-13**, Ninomiya et al. disclose every limitation as shown in claims 4-5 above and the limitation that (a) the circuitry layer and the metal layer release stress within 24 hours at 100°C and (b) elongation during rupture of the circuitry layer and the metal layer is from 20% to 30% within the range of -40°C to 150°C are interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art. Thus, Ninomiya et al. anticipate the claims.

**Regarding claims 14-16**, Ninomiya et al. disclose the thickness of the metal layer 9 has a thickness of at least 0.05 mm (column 8, lines 30-36) and layer 11 (which is in the same manner as metal layer 9) is also 0.5 mm (column 11, lines 18-19). But, Ninomiya et al. does not disclose the thickness of the circuit layer.

It is old and known in the art that the thickness of a circuit layer is depend upon a particular application, wherein in the range of 0.04 mm to 1.00 mm is well known in the art. Thus, it is merely a matter of choice depending on a specific application.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select the above range in order to meet a minimum requirement in electric current resistivity for a particular application. Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

**Regarding claims 17-19**, Ninomiya et al. disclose the conductivity of the circuitry layer and the metal layer is inherently at least 99% under IACS, since the material is copper of at least 99.99% in purity (considering at least 99.99% in purity, see example 2 in column 14) and also see claim 1 above. It is noted that the IACS set the conductivity of copper at 100%.

**Regarding claims 20-22**, Ninomiya et al. disclose every limitation as shown in claims 4-6 above, but failed to disclose that the average particle diameter of crystalline particles of the circuitry layer and the metal layer is from 1.0-30 mm.

Again, as clearly explained in claim 1 above, a selection of the best suitable material involves only routine skill in the art. It is also well known in the art that the grain size particle of a material dictates the material properties including toughness and brittleness of malleability, and its face transition point is also affected.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select the above range in order to increase the toughness of the circuitry layer and the metal layer. Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

### ***Response to Arguments***

6. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for




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published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen  
5/12/06



KAMAND CUNEO  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800